TOUIT, INC.

Touit Pro PCI Express Core

Datasheet
March, 2008

1. Features

- Complies with PCI Express Base Specification V1.1
- Complies with the PCI Express Architecture (PIPE) Specification V1.00
- Layered architecture with Configuration Space, Transaction Layer, Data Link Layer and Physical Layer
- Implements receive and transmit buffers, Flow Control (FC) and Transaction Ordering
- Implements the Message Signaled Interrupt, Power Management, Device Serial Number and PCI Express capability registers
- Optionally implements Virtual Channels and Advanced Error Reporting
- Supports up to 4 Virtual Channels
- Supports configurable maximum packet sizes in the range of 128B to 2KB
- Full Duplex communication
- Handles packet error detection and reporting
- Implements End-to-End Cyclic Redundancy Checking (ECRC)
- Up to 32 out standing requests with timeout control
- DMA controller, 2 channels with scatter gather
- Easy to use Application Layer Interface.

2. Description

The Touit PCI Express Pro Core provides a PCI Express Endpoint solution with easy to use Application Layer Interface. Freeing the user from all PCI Express implementation details. The Pro core will handle all Configuration Space requests and PCI Express packet checking rules. The core handles the Flow Control (FC) checking on both the receive and transmit lanes. It will allow up to 32 outstanding read request packets to be issued and implements a completion timer for each request. If the completion timer expires the core will resend the request. Advanced Error Reporting, Power Management and Message Signaled Interrupts are PCI Express functions also included in the core.

The Pro Core includes an intermediary layer between the Application Layer and the Transaction Layer. This Transaction Layer Packet (TLP) processing layer, or Pro Layer, handles all the overhead, detail and work related to the receipt and transmission of TLPs. This allows the user to focus exclusively on the actual application design instead of PCI Express fundamentals.

The Pro core is compliant to the PIPE interface for connection to PIPE compliant SERDES blocks. The core uses internal FPGA memory blocks for the Retry Buffer and Receive and Transmit buffers.

3. The Core

Configuration Space

The configuration space contains the register map for all the PCI Express configuration and status registers. It has an interface that provides read and write access to these registers for configuration read and write requests. A complete set of configuration and status registers are provided. These include:

- PCI Type 0 header for Endpoint mode
- Power Management Capability
- Message Signaled Interrupt Capability
- PCI Express Capability
- Virtual Channels Capability
- Advanced Error Reporting Capability

Any read accesses to addresses not implemented returns zeros and any writes are treated as No Ops.

The registers are set via access signals provided by the core.

The Transaction Layer handles any accesses to the configuration space through configuration requests and will generate the appropriate completions as required.

Pro Layer

The Pro Layer provides all the necessary handling for the successful receipt and transmission of TLPs. This provides an interface to the Application Layer free of any of the PCI Express funcational details and resembles a simple read and write interface. The Pro Layer initiates transactions through a DMA controller with scatter gather capabilty. When the Pro Layer receives requests from the PCI Express fabric, it will anaylze the requests and initiate a read or write transaction with the Application Layer. The Pro Layer will then finish the request after all data has been transferred with the Application Layer. There is a Operational Register (OPREG) block which provides control and status signals for the components in the Pro Layer.

Transaction Layer

The Transaction Layer is located between the Application Layer and the Data Link Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. Every TLP requiring a response packet is implemented as a split transaction between the receive and transmit sides of the Transaction Layer.

The transmit side of the Transaction Layer receives data from the Application Layer and forms TLPs, encapsulating the data, which are sent on to the Data Link Layer. Data is sent in either a write request TLP or in a completion TLP. The transmit side also sends read request TLPs when the Application Layer requests data. The Transaction Layer gives each read request TLP a unique identifier that enables completion TLPs to be directed to the originator of the request TLP. Each read request has a timer that monitors the read data returned via completion packets on the receive side of the Transaction Layer. The timer will reset when any of the requested data is received and will disable when the entire read transaction is completed. If the timer expires before the transaction completes, this is called a Completion Timeout. If enabled, on a Completion Timeout the read request will be resent by the Transaction Layer.

The receive side of the Transaction Layer receives TLPs from the Data Link Layer, analyzes the TLP and sends the data on to the Application Layer. The receive side also handles configuration space requests by issuing a read or write transaction to the configuration registers, and then schedules a completion packet to be sent with the transmit side of the Transaction Layer. If an error is detected in the TLP, the packet will be discarded and an error message will be scheduled for transmission to the root complex or host system.

The Transaction Layer is also responsible for managing credit-based Flow Control (FC) for TLPs. The amount of available space in the receive buffers determines the number of FC credits available. The Transaction Layer will hold-off any transaction waiting to be sent if there are not enough FC credits available on the other end of the link. Optional End-to-End Cyclic Redundancy Checking (ECRC) is done and generated in the Transaction Layer as well as Power Management events.

Data Link Layer

The Data Link Layer (DLL) is located between the Transaction Layer and the Physical Layer in a PCI Express link. It provides packet tracking and error control between the two ends of a PCI Express link. The DLL also initializes the flow control information for the link.

Data integrity for a packet is ensured through the use of a CRC appended to the end of each packet. Packet tracking is handled by adding and tracking sequence numbers on each packet. The DLL on each end of the link will exchange acknowledgment packets, called Data Link Layer Message (DLLM) ACK and NAK packets, to signal successful or unsuccessful receipt of data. The DLL implements a Retry Buffer to store transmitted packets for re-transmission if required. After the DLL receives an acknowledgment that the other end of the link has successfully received a packet, the DLL will remove that packet from the Retry Buffer.

If any errors are detected the DLL will alert the Transaction Layer.

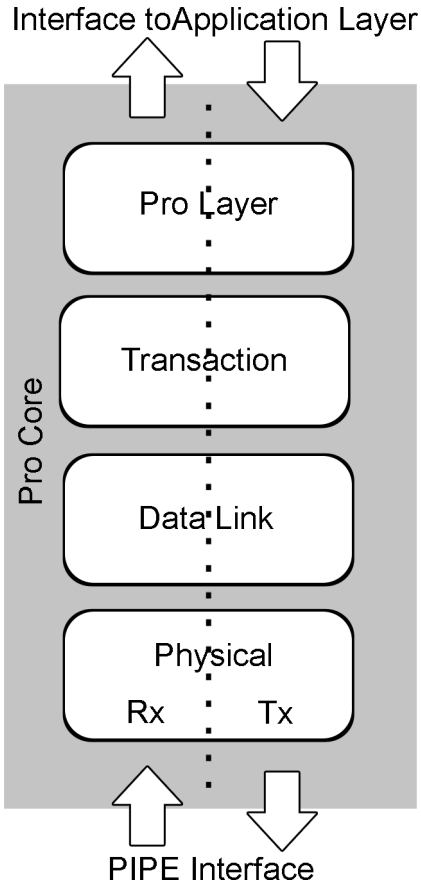
Physical Layer

The Physical Layer is located between the Data Link Layer and the SERDES or Phy. This layer is responsible for low level link management. The Physical Layer performs link initialization to establish lock and determine the width and speed of the link. After the link is initialized the Physical Layer will place specialized symbol characters before and after packets received from the Data Link Layer for transmission. These characters alert the Physical Layer on the receiving end of the link to the start and finish of a packet.

Lane to lane deskew and data scrambling/unscrambling are also implemented in the Physical Layer.

4. Core Block Diagram

Shown below is a simplified block diagram of the Pro PCI Express Core:



5. Signal Descriptions

PIPE Interface Signal Table

Signal Name	*I/O*	*Width*	*Description*
pcie_reset	I	1	PCI Express Bus reset signal.
pipe_reset	O	1	Resets the transmitter and receiver in the PHY.
pipe_tx_data	O	16	Parallel data output bus to the PHY.

Signal Name	*I/O*	*Width*	*Description*
pipe_tx_data_k	O	2	Data/Control for the symbols of transmit data. Bit 0 corresponds to the low-byte of pipe_tx_data, Bit 1 to the upper byte. A value of zero indicates a data byte, a value of 1indicates a control byte.
pipe_rx_data	I	16	Parallel data input bus from the PHY.
pclk	I	1	Parallel interface data clock. All data movement across the parallel interface is synchronized to this clock.
pipe_rx_data_k	I	2	Data/Control bit for the symbols of receive data. Bit 0 corresponds to the low-byte of pipe_rx_data, Bit 1 to the upper byte. A value of zero indicates a data byte; a value of 1 indicates a control byte.
pipe_tx_detect_loopback	O	1	Used to tell the PHY to begin a receiver detection operation or to begin loopback.
pipe_tx_elecidle	O	1	Forces PHY Tx output to electrical idle.
pipe_tx_compliance	O	1	Sets the running disparity to negative. Used when transmitting the compliance pattern.
pipe_rx_status	I	3	Encodes receiver status and error codes for the received data stream and receiver detection.
pipe_rx_polarity	O	1	Tells PHY to do a polarity inversion on the received data.
pipe_rx_elecidle	I	1	Indicates receiver detection of an electrical idle.
pipe_rx_valid	I	1	Indicates symbol lock and receipt of valid data.
pipe_powerdown	O	2	Power up or down the transceiver.
pipe_status	I	1	Used to communicate completion of several PHY functions including power management state transitions, and receiver detection.

Application Layer Interface Signal Table

Signal Name	*I/O*	*Width*	*Description*
local_opreg_ready	I	1	Initiates transfer between local interface and OPREGs
local_opreg_rdwr	I	1	Idicates direction of transfer. High read, low write.
local_opreg_enable	O	1	Signals succesful transfer of data on data port.

Signal Name	*I/O*	*Width*	*Description*
local_opreg_last	I	1	Indicates last data transfer.
local_opreg_addr	I	8	Address to the first register in transfer. In a multi-cycle data transfer, subsequent data transfers will be to or from OPREGS in ascending order from the address provided.
local_opreg_di	I	32	Write data port.
local_opreg_do	O	32	Read data port.
local_wr_ready	O	1	Initiates write transfer to local interface.
local_wr_enable	I	1	Signals succesful transfer of data on write data port.
local_wr_last	O	1	Indicates last data of write transfer.
local_wr_addr	O	32	First address location in write transfer.
local_wr_data	O	32	Write data port.
local_rd_ready	O	1	Initiates read transfer from local interface.
local_rd_enable	I	1	Signals succesful transfer of data on read data port.
local_rd_last	O	1	Indicates last data of read transfer.
local_rd_addr	O	32	First address location in read transfer.
local_rd_data	I	32	Read data port.
pcie_interrupt	I	1	Send interrupt to the root complex.

Configuration Space Signal Table

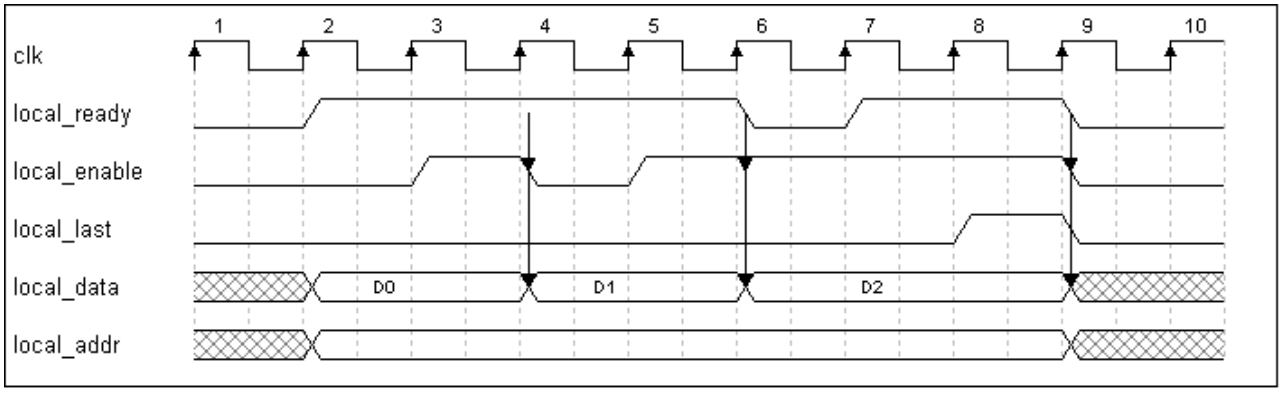
These values should not be changed after system initialization. It is recommended that these values be harcoded in the HDL.

Signal Name	*I/O*	*Width*	*Description*
bar_x_enable	I	1	Enables the Base Address Register (BAR) in configuration space. NOTE: only BARs 0, 2, and 4 are available for use as memory space. BAR 1, 3, and 5 are reserved for use when BAR 0, 2, or 4 are set to 64 bit address mode. BAR x+1 is the upper 32 bit address value for BAR x. Where 'x' is 0, 2, or 4.
bar_x_64bit	I	1	Sets BAR to 64 bit address mode.
bar_x_size	I	25	Sets the size of the address region in bytes.
bar_x	O	25	Address assigned to BAR.
bar_x+1_size	I	32	Sets the size of the upper 32 bit address region.

Signal Name	*I/O*	*Width*	*Description*
bar_x+1	O	32	Address assigned to BAR.

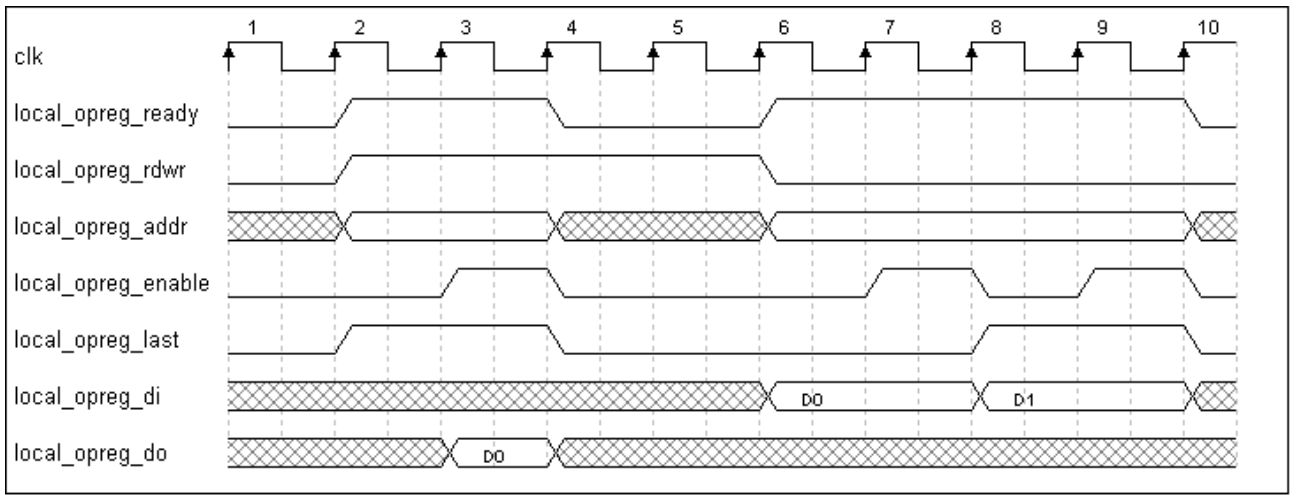
6. Timing Diagrams

Local Read or Write Interface to the Application Layer:



As shown in the diagram above, both the enable and ready signals are capable of holding off the data bus. This allows both the Pro Layer and the Application Layer the ability to throttle the data transfer.

Local Operational Register Interface to the Application Layer:



For the OPREG interface between the Pro Layer and the Application Layer, only the Pro Layer can hold off either the input or output data buses.

7. Operational Register Address Map

NOTE: All PCI Express initiated requests to the OPREGS must be addressed to BAR0. All the addresses listed are offset from BAR0.

Register Name	*PCIe Address*	*Local Address*	*Description*
IntCSR	0x00	0x00	Interrupt control and status register.
Dma0CSR	0x10	0x10	Dma Channel 0 configuration and status register.
Dma0Addr	0x11	0x11	Dma Channel 0 PCI address register.
Dma0LAddr	0x12	0x12	Dma Channel 0 Local address register.
Dma0Length	0x13	0x13	Dma Channel 0 transfer length.
Dma0Dptr	0x14	0x14	Dma Channel 0 description pointer.
Dma0uprAddr	0x15	0x15	Dma Channel 0 PCI address register. Upper 32 bits for a 64 bit mode transfer.
Dma1CSR	0x20	0x20	Dma Channel 1 configuration and status register.
Dma1Addr	0x21	0x21	Dma Channel 1 PCI address register.
Dma1LAddr	0x22	0x22	Dma Channel 1 Local address register.
Dma1Length	0x23	0x23	Dma Channel 1 transfer length.
Dma1Dptr	0x24	0x24	Dma Channel 1 description pointer.
Dma1uprAddr	0x25	0x25	Dma Channel 1 PCI address register. Upper 32 bits for a 64 bit mode transfer.
BA2LAddr	0x30	0x30	Base Address 2 region to local address translation register.
BA4LAddr	0x31	0x31	Base Address 4 region to local address translation register.

8. Register Bit Field Descriptions

Interupt Control and Status Register

Bit	*Description*	*Read*	*Write*	*Value after Reset*
0	PCI Express interrupt enable.	Yes	Yes	0
1	Local interrupt signal source enable. A value of 1 indicates this signal is a valid source to trigger PCI Express interupts.	Yes	Yes	0
2	DMA Channel 0 source enable. A value of 1 indicates this signal is a valid source to trigger PCI Express interupts.	Yes	Yes	0
3	DMA Channel 1 source enable. A value of 1 indicates this signal is a valid source to trigger PCI Express interupts.	Yes	Yes	0
15:4	Reserved	Yes	No	0
16	Local interupt signal line active.	Yes	No	0
17	DMA Channel 0 interupt active.	Yes	No	0
18	DMA Channel 1 interupt active.	Yes	No	0
31:19	Reserved	Yes	No	0

DMA Channel X Control and Status Register (X = 0 or 1)

Bit	*Description*	*Read*	*Write*	*Value after Reset*
0	DMA Channel enable. Writing a 1 to this bit location will enable the DMA channel to do transfers.	Yes	Yes	0
1	DMA Channel start. Writing a 1 to this bit location will signal the DMA channel to begin a transfer. Writing a 0 to this location has no effect and reading from this location will always return a 0.	Yes	Yes	0
2	DMA Channel clear. Writing a 1 to this bit location will clear the last DMA transfer. Clearing the last DMA transfer will deassert the DMA channel done and interupt signals, and will put the channel in a ready state to start new transfers. A write of 0 and then 1 to the DMA channel enable	Yes	Yes	0

Bit	Description	Read	Write	Value after Reset
	bit location (bit 0) will have the same effect as a write of 1 to the DMA channel clear bit. Writing a 0 to this location has no effect and reading from this location will always return a 0.			
3	DMA Channel done signal. A value of 1 indicates the last DMA transfer has completed.	Yes	No	0
4	DMA Cannel scatter/gather enable. Setting this bit to 1 will instruct the DMA channel to perform a scatter/gather DMA transfer. After the initial DMA transfer completes, it will reload the DMA registers by reading from the loacation pointed to by the DMAxDptr register. If this bit is set to 0 then the DMA channel will perform a single Block DMA transfer.	Yes	Yes	0
5	DMA Channel done interrupt enable. Setting this bit to 1 will cause an interrupt to be sent to the root complex when the DMA transfer completes. NOTE: The interrupt will not be sent to the root complex if the other PCI Express interrupt enables are not properly configured.	Yes	Yes	0
6	Local address mode. A value of 1 will hold the local address value constant throughout an entire scatter/gather DMA transaction. A value of 0 will cause it to be incremented.	Yes	Yes	0
31:7	Reserved	Yes	No	0

DMA Channel X PCI Express Address Register (X = 0 or 1)

Bit	Description	Read	Write	Value after Reset
1:0	Reserved	Yes	No	0
31:2	PCI Express address from which the DMA channel will read or write.	Yes	Yes	0

DMA Channel X Local Address Register (X = 0 or 1)

Bit	Description	Read	Write	Value after Reset
31:0	Local DWORD address from which the DMA channel will read or write.	Yes	Yes	0

DMA Channel X Transfer Length Register (X = 0 or 1)

Bit	*Description*	*Read*	*Write*	*Value after Reset*
22:0	DMA transfer length in DWORDs.	Yes	Yes	0
31:23	Reserved	Yes	No	0

DMA Channel X Description Pointer Register (X = 0 or 1)

Bit	*Description*	*Read*	*Write*	*Value after Reset*
0	DMA Channel end-of-chain bit location. A value of 1 sets the current DMA transfer to be the final transfer in the DMA scatter/gather transfer. This field has no effect on DMA Block transfers.	Yes	Yes	0
1	DMA Channel transfer direction. A value of 1 indicates a Local to PCI Express transaction and a 0 indicates a PCI Express to Local transaction.	Yes	Yes	0
3:2	Reserved	Yes	No	0
31:4	Address location for the next DMA scatter/gather transfer descriptor. The address is aligned to a 32 byte boundary. A descriptor consists of all the DMA channel opregs except for the DmaXCSR register. A DMA descriptor contains the following register values offset from the current value in DmaXDptr(31:4) : 0x0 - DmaXAddr 0x1 - DmaXLAddr 0x2 - DmaXLength 0x3 - DmaXDptr 0x4 - DmaXuprAddr	Yes	Yes	0

DMA Channel X Upper PCI Express Address Register (X = 0 or 1)

Bit	*Description*	*Read*	*Write*	*Value after Reset*
31:0	DMA Channel PCI Express address register for the upper 32 bits in 64 bit address mode.	Yes	Yes	0

Base Address to Local Address Translation Registers

Bit	***Description***	***Read***	***Write***	***Value after Reset***
31:0	The value in this register sets the local address value corresponding to the value set in the Configuration Space BAR. The range for the local address will be the same as the range set for the BAR.	Yes	Yes	0